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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/993,415	11/05/2001	Thomas Boehler	01 P 16795 US	6857

7590 06/16/2004

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EXAMINER	
DOOLEY, MATTHEW C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 06/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/993,415	BOEHLER ET AL.	
	Examiner	Art Unit	
	Matthew C. Dooley	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 November 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-24* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 November 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 7 recites the limitation "the stored bits" in line 6 of page 13. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3-9, 11-13, 15-20, 22-24 are rejected under 35 U.S.C. 102(e) as being anticipated by Vollrath et al., U.S. 6,564,346.

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37 CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

As per claim 1:

Vollrath teaches to obtaining test information for a group of memory locations within a memory apparatus, compressing the test information to produce compressed test information, and based on the compressed test information, replacing a group of redundant memory circuits associated with the memory locations (Fig.8; Col.2: 23-29; Col.13: 15-26).

As per claim 3:

The group of memory locations is a group of neighboring memory cells in a DRAM array (Col.3: 50; Fig.1b).

As per claim 4:

The group of memory cells is a group of neighboring memory cells in a single row of the DRAM array (Fig.1d).

As per claim 5:

The compressing step includes storing the test information for each of the memory locations in a corresponding storage location (Col.11: 1-5).

As per claim 6:

The test information for each of the memory locations of the group is a corresponding bit which is indicative of whether the associated memory location has failed a memory test (Col.11: 1-30).

As per claim 7:

Vollrath teaches to logically combining the stored bits (Col.11: 53-59).

As per claim 8:

The logically combining step of Vollrath includes logically ORing the stored bits (Col.11: 55).

As per claim 9:

Vollrath teaches to obtaining test information for each memory location of a plurality of groups of memory locations and compressing the test information respectively associated with each of the groups to produce compressed test information (Col.11: 5-42).

As per claim 11:

Vollrath teaches to the replacement of redundant memory circuits when the compressed test information indicates that at least one of the group of memory locations has failed (Fig.8; Col.12: 1-5).

As per claim 12:

The group of memory locations of Vollrath is a group of neighboring memory cells in a DRAM array, and the replacing includes replacing redundant bitlines associated with the neighboring memory cells of the DRAM array (Col.2: 23-29; Col.3: 50; Fig.1b; Fig.8; Col.12: 1-5).

As per claim 13:

Claim 13 is the apparatus claim corresponding to method claim 1 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 1 above.

As per claim 15:

Claim 15 is the apparatus claim corresponding to method claim 5 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 5 above.

As per claim 16:

Vollrath teaches to a routing apparatus that routs test information for each of the memory locations to its corresponding storage location (Col.10: 57 – Col.11: 5).

As per claim 17:

Claim 17 is the apparatus claim corresponding to method claim 6 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 6 above.

As per claim 18:

Claim 18 is the apparatus claim corresponding to method claim 7 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 7 above.

As per claim 19:

Claim 19 is the apparatus claim corresponding to method claim 8 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 8 above.

As per claim 20:

Claim 20 is the apparatus claim corresponding to method claim 9 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 9 above.

As per claim 22:

Claim 22 is the apparatus claim corresponding to method claim 11 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 11 above.

As per claim 23:

Vollrath teaches to a tester responsive to the compressed test information for determining whether to replace the redundant memory circuits (Col.10: 46 – Col.11: 5; Col.12: 1-5).

As per claim 24:

Claim 24 is the apparatus claim corresponding to method claim 12 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 12 above.

5. Claims 1-2, 13-14 rejected under 35 U.S.C. 102(e) as being anticipated by Takano et al., U.S. 6,374,378.

As per claim 1:

Takano teaches to obtaining test information for a group of memory locations within a memory apparatus, compressing the test information to produce compressed test information, and based on the compressed test information, replacing a group of redundant memory circuits associated with the memory locations (Abstract; Fig.7; Col.1: 60-67; Col.2: 12-30).

As per claim 2:

Takano teaches to comparing information stored in said memory locations to corresponding expected information stored in said memory locations (Col.4: 35-50).

As per claim 13:

Claim 13 is the apparatus claim corresponding to method claim 1 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 1 above.

As per claim 14:

Claim 14 is the apparatus claim corresponding to method claim 2 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 2 above.

6. Claims 1-2, 13-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Merritt et al., U.S. 6,484,278.

As per claim 1:

Merritt teaches to obtaining test information for a group of memory locations within a memory apparatus, compressing the test information to produce compressed test information, and based on the compressed test information, replacing a group of redundant memory circuits associated with the memory locations (Abstract; Fig.2; Col.2: 58 – Col.3: 19; Col.6: 65 – Col.7: 4).

As per claim 2:

Merritt teaches to comparing information stored in said memory locations to corresponding expected information stored in said memory locations (Abstract; Fig.2; Col.2: 58 – Col.3: 19).

As per claim 13:

Claim 13 is the apparatus claim corresponding to method claim 1 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 1 above.

As per claim 14:

Claim 14 is the apparatus claim corresponding to method claim 2 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 2 above.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 10, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Takano et al., U.S. 6,374,378, in view of Schicht, U.S. 6,163,863, and Pyle, U.S. 5,418,452.

As per claim 10:

Takano fails to teach to time division multiplexing the compressed test information for input to a tester separate from the memory apparatus. Schicht teaches to the use of multiplexing circuitry in conjunction with compressed test information (Fig.3). Pyle teaches to the use of time division multiplexing test information to a tester that is physically separate from the memory apparatus (Fig.1). It would have obvious for one of ordinary skill in the art at the time of the invention to make use of the use of multiplexing circuitry in conjunction with compressed test information for use with time division multiplexing test information to a tester that is physically separate from the memory apparatus in conjunction with the system of Takano because the observable test nodes can be increased without increasing the number of necessary pins on an IC chip (Pyle: Col.2: 51-56).

As per claim 21:

Claim 21 is the apparatus claim corresponding to method claim 10 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 10 above.

9. Claims 10, 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Merritt et al., U.S. 6,484,278, in view of Schicht, U.S. 6,163,863, and Pyle, U.S. 5,418,452.

As per claim 10:

Merritt fails to teach to time division multiplexing the compressed test information for input to a tester separate from the memory apparatus. Schicht teaches to the use of multiplexing circuitry in conjunction with compressed test information (Fig.3). Pyle teaches to the use of time division multiplexing test information to a tester that is physically separate from the memory apparatus (Fig.1). It would have obvious for one of ordinary skill in the art at the time of the invention to make use of the use of multiplexing circuitry in conjunction with compressed test information for use with time division multiplexing test information to a tester that is physically separate from the memory apparatus in conjunction with the system of Merritt because the observable test nodes can be increased without increasing the number of necessary pins on an IC chip (Pyle: Col.2: 51-56).

As per claim 21:

Claim 21 is the apparatus claim corresponding to method claim 10 and as such is rejected under analogous reasoning as that set forth in the rejection of claim 10 above.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Bunker U.S. 6,311,299

b. Wang et al. U.S. 6,543,015

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew C. Dooley whose telephone number is (703) 306-5538. The examiner can normally be reached on M-F 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Matthew Dooley
Examiner AU 2133
06/10/04

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